Patent Claims

1. A base semiconductor component for a semiconductor component stack (2) comprising a semiconductor chip (3) arranged on a stiff wiring substrate (4), wherein
   - the wiring substrate (4) has contact pads (8) on its upper side (5) in edge regions (6, 7) and external contacts (10) of the base semiconductor component (1) on its underside (9) opposite to the semiconductor chip (3);
   - contact areas of an integrated circuit of the active upper side (11) of the semiconductor chip (3) and/or the external contacts (10) together with the contact pads (8) are electrically connected to one another via wiring lines (12) and/or through contacts (13) of the wiring substrate (4);
   - a deformable interconnection film (14) defines the upper side (15) of the base component and has a freely accessible arrangement pattern (16) of stack contact areas (17) arranged congruently with respect to external contacts (18) of a semiconductor component (19) to be stacked;
   - the interconnection film (14) is deformed in its edge regions (20, 21) toward the contact pads (8) of the wiring substrate (4); and wherein
   - the stack contact areas (17) are electrically connected to the contact pads (8) of the wiring substrate (4) via conductor tracks (22) of the interconnection film (14).

2. The base semiconductor component as claimed in claim 1,
characterized in that

the semiconductor chip (3) has flip-chip contacts (23) which are connected via wiring lines (12) to the contact pads (8), and via wiring lines (12) on the upper side (5) and through contacts (13) to the underside (9) of the wiring substrate (4), and also via wiring lines (12) on the underside (9) of the wiring substrate (4) to external contact areas (24), the external contact areas (24) having the external contacts (10).

3. The base semiconductor component as claimed in claim 2,
characterized in that
the external contacts (10) have solder balls and are arranged on the underside (9) of the wiring substrate (4) in a matrix.

4. The base semiconductor component as claimed in one of the preceding claims,
characterized in that
the interconnection film (14) is concomitantly arranged on the rear side (25) of a base semiconductor chip (3).

5. The base semiconductor component as claimed in one of the preceding claims,
characterized in that
a supporting plate (26) is arranged between the interconnection film (14) and the semiconductor chip (3).

6. The base semiconductor component as claimed in one of the preceding claims,
characterized in that
the base semiconductor component (1) and the stacked semiconductor component (19) are electrically connected via the stack contact areas (17) of the interconnection film (14).

7. The base semiconductor component as claimed in one of the preceding claims, characterized in that the interconnection film (14) has a plurality of mutually insulated layers with conductor tracks (22).

8. The base semiconductor component as claimed in one of the preceding claims, characterized in that the semiconductor chip (3) of the base semiconductor component (1) is embedded in a plastics composition (27).

9. The base semiconductor component as claimed in one of the preceding claims, characterized in that the semiconductor chip (3) of the base semiconductor component (1) is electrically connected to the contact pads (8) via bonding wire connections.

10. The base semiconductor component as claimed in one of the preceding claims, characterized in that the connection locations between contact pads (8) and conductor tracks of the interconnection film (14), in the edge regions (6, 7) of the wiring substrate (4), are embedded in a plastic covering (28).

11. A method for the production of a base semiconductor component (1) has the following method steps:

- production of a stiff wiring carrier (4) with a central semiconductor chip (3) on its upper side (5) and contact pads (8) in edge regions

(6, 7) of the upper side (5), and also external contact areas (24) on its underside (9), the external contact areas (24) and the contact pads (8) and also contact areas of an integrated circuit of the semiconductor chip (3) being electrically connected to one another;

- production of a deformable interconnection film (14) with stack contact areas (17) on its upper side (15), which have an arrangement pattern (16) that is congruent with respect to an arrangement pattern of external contacts (18) of a semiconductor component (19) to be stacked, and with conductor tracks (22) on its underside (9), which are connected to the stack contact areas (17) and extend right into the edge regions (20, 21) of the intermediate carrier film (14), the conductor tracks (22) having an arrangement pattern that is congruent with respect to the arrangement pattern of the contact pads (8);
- application of the interconnection film (14) by its underside (9) onto the wiring carrier (4) with semiconductor chip (3);
- deformation of the edge sides (20, 21) of the interconnection film (14) with the conductor tracks (22) being connected to the contact pads (8).

12. The method as claimed in claim 11, characterized in that before the interconnection film (14) is applied onto the wiring substrate (4), a supporting plate (26) is applied onto the underside (9) of the interconnection film (14).

13. The method as claimed in claim 11 or claim 12, characterized in that

before the interconnection film (14) is applied, the semiconductor chip (3) is embedded in a plastics composition (27).

14. The method as claimed in one of claims 11 to 13, characterized in that
after the conductor tracks (22) have been connected to the contact pads (8), the connection locations are embedded in a plastic covering (8).